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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,134	03/25/2002	Kent Kuohua Chang	MXIP0079USA	5974

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER	
DEO, DUY VU NGUYEN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,134	CHANG ET AL.	
	Examiner	Art Unit	
	DuyVu n Deo	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 2, 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeng (US 6,391,718).

Jeng describes a method to form a flash memory device comprising: providing a stacked layer of polysilicon layer and a cap layer of silicon nitride (claimed sacrificial layer) on a substrate (col. 3, line 10-21); (since this is the same device as claimed invention, flash memory device, the substrate where the stacked layer is formed would be the claimed channel region and substrate surface between the stacked layer would be the claimed bit line); depositing a dielectric layer of silicon dioxide by HDP-CVD to cover the channel and bit line regions, the top surface of

the silicon dioxide within the bit line region being above the top surface of the polysilicon layer and below the silicon nitride layer (col. 3, line 21-26; figure 1A); wet etching (claimed isotropically etching: please also cited Wolf below) away a portion o the silicon dioxide layer to expose a portion of the silicon nitride layer, and at the same time diving the silicon dioxide layer into a first silicon dioxide portion positioned on the silicon nitride layer and a second silicon dioxide portion that is not connected with the first silicon dioxide portion (col. 3, line 26-32; figure 1B); removing the first silicon dioxide portion and the silicon nitride layer (col. 3, line 59-col. 4, line 5).

Referring to claim 5, since the second silicon dioxide layer has a protrusion structure near the polysilicon layer, which is the same as that of the claimed invention, it would also provide claimed increasing GCR of the flash memory.

Referring to claim 6, the silicon nitride layer is removed by a wet etching using hot phosphoric acid (col. 4, line 1-5).

3. Claims 1-6, 9-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu et al. (US 6,576,514).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Liu describes a method to form a flash memory device comprising: providing a stacked layer of polysilicon layer and a cap layer of silicon nitride (claimed sacrificial layer) on a substrate (col. 3, line 35-39); (since this is the same device as claimed invention, flash memory device, the substrate where the stacked layer is formed would be the claimed channel region and substrate surface between the stacked layer would be the claimed bit line); depositing a dielectric layer of silicon oxide by HDP-CVD to cover the channel and bit line regions, the top surface of the silicon oxide within the bit line region being above the top surface of the polysilicon layer and below the silicon nitride layer (col. 4, line 30-39; figure 11); wet etching (claimed isotropically etching: please also cited Wolf below) away a portion o the silicon oxide layer to expose a portion of the silicon nitride layer using heated phosphoric acid, and at the same time diving the silicon oxide layer into a first silicon oxide portion positioned on the silicon nitride layer and a second silicon oxide portion that is not connected with the first silicon oxide portion (col. 4, line 40-43; figure 12; claim 12); removing the first silicon oxide portion and the silicon nitride layer (col. 4, line 50-55).

Referring to claim 9, the method for forming the flash memory further comprising: forming a second polysilicon layer over the first polysilicon layer so that the first and second polysilicon layers forming a floating gate for the flash memory, forming an ONO film over the floating gate, and forming a third polysilicon layer over the ONO layer (col. 3, line 60-col 4, line 6).

Referring to claims 3 and 12, the bit line region is doped to serve as a buried source or drain (col. 3, line 33-39).

Referring to claims 5 and 14, since the second silicon oxide layer has a protrusion structure near the polysilicon layer, which is the same as that of the claimed invention, it would also provide claimed increasing GCR of the flash memory.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng as applied to claims 1 above, and further in view of Su (US 6,569,735).

Referring to claims 3, 9, and 12, Jeng is silent about the steps of doping the region adjacent to the polysilicon layer in the bit line region to form a buried source or drain, forming a second polysilicon layer over the first polysilicon layer so that the first and second polysilicon layers forming a floating gate for the flash memory, forming an ONO film over the floating gate, and forming a third polysilicon layer over the ONO layer. However, these steps are well known to one skill in the art as shown here by Su (col. 4, line 9-15, line 41-61). It would have been obvious for one skill at the time of the invention in light of Su's steps to perform those extra steps cited above because they both teaches steps for forming flash memory device and Su further describes steps that are silent in Jeng in order to form a flash memory device with a reasonable expectation of success.

6. Claims 7, 8, 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng or Jeng/Su or Liu as applied to claims 1 and 9 above.

Referring to claims 7, 8, 17, 18, applied prior art of Jeng, Liu or Jeng/Su doesn't describe the thickness of the silicon dioxide being isotropically etched is about 450-750 or about 600 angstrom. However, it would have been obvious to one skill in the art at the time of the invention that the thickness being etched would have be to determined through test runs so that a appropriate thickness can be removed in order to expose a portion of the silicon nitride and to form a first and second separated silicon dioxide layer.

7. Wolf et al. is cited to show prior art, page 529.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,576,514. Although the conflicting claims are not identical, they are not patentably distinct from each other because they

both teaches similar steps for forming flash memory device having dielectric layer formed in the bit line region.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 703-305-0515.

DVD
11/17/03